Computer Architecture / Course Description

1. Course Name:

Computer Architecture

2. Course Code:

CSCL3224

3. Semester / Year:

Third

4. Description Preparation Date:

Each year there is a minor modification to be up to date (5-2-2024)

5. Available Attendance Forms:

theoretical and practical

6. Number of Credit Hours (Total) / Number of Units (Total)

4 hours weekly (2 theoretical and 2 practical) totally 4*15 = 60 hours
Units=3

7. Course administrator's name (mention all, if more than one name)

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8. Course Objectives

Course Objectives	1. To impart basic concepts of computer architecture and organization, 2. To explain key skills of constructing cost-effective computer systems. 3. To familiarize the basic CPU organization. 4. To help students in understanding various memory devices. To facilitate students in learning IO communication

9. Teaching and Learning Strategies

Strategy	The main strategy that will be adopted in delivering this module is to encourage students' participatio in the exercises, while at the same time refining and expanding their critical thinking skills. This will b achieved through classes, interactive tutorials and by considering type of simple experiments involvin some sampling activities that are interesting to the students.

10. Course Structure

Week	Hours	Required Learning Outcomes	Unit or subject name	Learning method	Evaluation method
1	4	1,2,3, and 4	INTRODUCTION COMPUTER ARCHITECTURE	Presentation writing board	Formative/ Summative assessment

2	**4**	**1,2,3, and 4**	**STRUCTURE OF COMPUTERS**	**Presentation writing board**	**Formative/ Summative assessment**
3	**4**	**1,2,3, and 4**	Performance, Multiprocessor and Multicomputer, Data representation, Fixed and Floating point, Error detectio and correction codes	**Presentation writing board**	**Formative/ Summative assessment**
4	**4**	**1,2,3, and 4**	BASIC COMPUTER ORGANIZATION AND DESIGN:	**Presentation writing board**	**Formative/ Summative assessment**
5	**4**	**1,2,3, and 4**	Timing and Control, Memory Reference Instructions, Input Output and interrupt. Central processing unit:	**Presentation writing board**	**Formative/ Summative assessment**
6	**4**	**1,2,3, and 4**	Stack organization, Instructio Formats, Addressing Modes, Data Transfer and Manipulati Complex Instruction Set Computer (CISC) Reduced Instruction Set Computer (RISC), CISC vs RISC	**Presentation writing board**	**Formative/ Summative assessment**
7	**4**	**1,2,3, and 4**	**REGISTER TRANSFER AND MICRO-OPERATIONS** Register Transfer Language, Register Transfer, Bus and Memory Transfers,	**Presentation writing board**	**Formative/ Summative assessment**
8	**4**	**1,2,3, and 4**	**REGISTER TRANSFER AND MICRO-OPERATIONS** Arithmetic Micro-Operati Logic Micro-Operations, S Micro-Operations, Arithm logic shift unit.	**Presentation writing board**	**Formative/ Summative assessment**
9	**4**	**1,2,3, and 4**	**MICRO-PROGRAMMED CONTROL:** Control Memory, Add Sequencing	**Presentation writing board**	**Formative/ Summative assessment**
10	**4**	**1,2,3, and 4**	**MICRO-PROGRAMMED CONTROL:** Micro-Program example, sin design of Control Unit.	**Presentation writing board**	**Formative/ Summative assessment**
11	**4**	**1,2,3, and 4**	**MEMORY SYSTEM:** Memory Hierar Semiconductor Memo RAM(Random Access Memo	**Presentation writing board**	**Formative/ Summative assessment**
12	**4**	**1,2,3, and 4**	**MEMORY SYSTEM:** Memory Hierarchy, Semiconductor Memories, RAM(Random Access Memory),	**Presentation writing board**	**Formative/ Summative assessment**

12	**4**	**1,2,3, and 4**	**MEMORY SYSTEM:** Read Only Memory (ROM), Types of ROM, Cache Memory, Performance considerations, Virtual memory, Paging, Secondary Storage, RAID.	**Presentation writing board**	**Formative/ Summative assessment**
13	**4**	**1,2,3, and 4**	**INPUT OUTPUT:** I/O interface, Programmed IO, Memory Mapped IO, Interrupt Driven IO, DMA	**Presentation writing board**	**Formative/ Summative assessment**
14	**4**	**1,2,3, and 4**	**MULTIPROCESSORS:** Characteristics of multiprocessors, Interconnection structures, Inter Processor Arbitration, Inter processor Communication and Synchronization, Cache Coherence.	**Presentation writing board**	**Formative/ Summative assessment**

11.Course Evaluation

15 degrees practical
15 degrees Mid exam
10 degrees evaluating the attendance and activities of homework
60 degrees for final exam

12.Learning and Teaching Resources

Required textbooks (curricular boo if any)	M. Moris Mano (2006), Computer System Architecture, 3rd edition, Pearson/PHI, India
Main references (sources)	Anrew S. Tanenbaum (2006), Structured Computer Organization, 5th edition, Pearson Education Inc,
Recommended books and references (scientific journals, reports...)	1. Carl Hamacher, Zvonks Vranesic, SafeaZaky (2002), Computer Organization, 5th edition, McGraw Hill, New Delhi, India. 2. William Stallings (2010), Computer Organization and Architecture- designing for performance, 8th edition, Prentice Hall, New Jersy. 3. Anrew S. Tanenbaum (2006), Structured Computer Organization, 5th edition, Pearson Education Inc, John P. Hayes (1998), Computer Architecture and Organization, 3rd edition, Tata McGrawHill
Electronic References, Websites	William Stallings (2010), Computer Organization and Architecture- designing for performance, 8th edition, Prentice Hall, New Jersy.