	Ministry of Higher Education and Scientific Research - Iraq University of Technology Department of Computer Sciences Information System Branch	

MODULE DESCRIPTOR FORM
نموذج وصف المادة الدراسية

Module Information
معلومات المادة الدراسية

Module Title	**COMPUTER ORGANIZATION AND LOGIC DESIGN**	**Module Delivery**	
Module Type	BASIC	**Theory** **Lecture** **Lab** **Tutorial** **Practical** **Seminar**	
Module Code	COLD123		
ECTS Credits	6		
SWL (hr/sem)	150		

Module Level	1	**Semester of Delivery**	2
Administering Department	Type Dept. Code	**College**	Type College Code
Module Leader	Enas Tariq	**e-mail**	Enas.T.Khudir@uobaghdad.edu.iq
Module Leader's Acad. Title	Lecturer	**Module Leader's Qualification**	Msc
Module Tutor	None	**e-mail**	None
Peer Reviewer Name		**e-mail**	
Review Committee Approval		**Version Number**	

Relation With Other Modules
العلاقة مع المواد الدراسية الأخرى

Prerequisite module	None	**Semester**	

Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents
أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية

Module Aims أهداف المادة الدراسية	1. 1-To gain proficiency in using computer hardware and software. 2. 2-To become familiar with various digital technologies and tools. 3. 3-To help individuals increase their productivity, improve their communication abilities, enhance their problem-solving skills, and gain access to a wide range of information and resources available on the internet. 4. To introduce students to the fundamental concepts and principles of logic design. 5. To develop students' skills in designing and analyzing digital logic circuits. 6. To enable students to apply logic design techniques to solve practical engineering problems. 7. To enhance students' understanding of the relationship between logic design and computer architecture.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	By the end of this module, students should be able to: 1. Understand the basic principles of Boolean algebra and logic gates. 2. Design, analyze, and optimize combinational logic circuits. 3. Design, analyze, and optimize sequential logic circuits. 4. Utilize programmable logic devices (PLDs) and field-programmable gate arrays (FPGAs) for logic design. 5. Apply simulation and verification techniques to validate the functionality of logic circuits. 6. Understand the role of logic design in computer architecture and digital systems.
Indicative Contents المحتويات الإرشادية	**Computer Organization:-** Evolution of Computers, Generation of Computers, Super Computers, Mainframe Computers, Personal Computers (Different Types) and Terminals (Different Types), Classification of Computers Analog Digital and Hybrid Computers, Classification of Computers according to size, Characteristics of Computers, Block Diagram of a Digital Computer. Operating systems (OS) , Types of OS, Dos and Windows operating system. Input Devices (Mouse, Keyboard...) Output Devices (Printers, VDU, ……) Motherboard, Microprocessor (Central Processing Unit (CPU)), Input / Output Ports Unit, Buses, BIOS, Memory types, and Storage units. Data and information. Data representation in computers, Different number systems (Decimal, Binary, Octal, and Hexadecimal), 1's Complement and 2's complement, Floating Point numbers, Coding – ASCII. Types of

	Programming Languages, software, Classification of software, Application software and System Software, Structured Programming, Algorithms and Flowcharts with Examples. **Logic Design:-** 1.Introduction to Logic Design . Overview of digital systems and their components . Binary number systems and codes . Boolean algebra and logic operations 2.Logic Gates and Combinational Logic Circuits . Basic logic gates (AND, OR, NOT, etc.) and their truth tables . Simplification techniques (Boolean algebra, Karnaugh maps) . Combinational logic circuits (adders, multiplexers, decoders, etc.) . Timing analysis and hazards in combinational circuits 3.Sequential Logic Circuits . Flip-flops, latches, and registers . Analysis and design of sequential circuits (state machines) . Synchronous and asynchronous sequential circuits . Timing considerations and clocking methodologies 4.Programmable Logic Devices (PLDs) and FPGAs . Introduction to PLDs and FPGAs . Implementation of logic circuits using PLDs and FPGAs . Configuration programming and hardware description languages (HDLs) 5.Simulation and Verification . Simulation tools for logic design (e.g., VHDL, Verilog) . Functional and timing simulation . Verification techniques (testbenches, formal verification) 6. Logic Design and Computer Architecture . Relationship between logic design and computer architecture . Introduction to processor design and memory systems . Logic design considerations for high-performance systems
Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	1. Conceptual Understanding: Focus on explaining fundamental concepts and principles of logic design, such as Boolean algebra, logic gates, and truth tables. 2. Visual Representations: Utilize diagrams and flowcharts to visually illustrate the structure and behavior of logic circuits. 3. Hands-on Activities: Provide opportunities for students to design and implement logic circuits using simulation software, breadboards, or hardware platforms. 4. Problem Solving: Assign problem-solving exercises and assignments that require students to analyze, design, and optimize logic circuits. 5. Real-World Applications: Relate logic design concepts to practical applications in computer processors, digital systems, and electronic

	devices. 6.Group Collaboration: Encourage collaborative learning through group projects and activities to foster teamwork and communication skills. 7. Simulation and Verification: Use logic simulation software or hardware description languages to simulate and verify logic circuits' functionality. 8. Error Analysis: Discuss common errors in logic design and guide students in identifying and rectifying mistakes in their designs. 9. Industry Practices: Introduce students to industry-standard design practices, tools, and methodologies used in logic design. 10. Assessment and Feedback: Regularly assess students' understanding through quizzes and provide constructive feedback to guide their learning and improvement..

Student Workload (SWL)
الحمل الدراسي للطالب

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	3.4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	LO # 5, 8 and 10
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7	LO # 1-7
	Final Exam	2hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction to computer architecture , Computer definition, History of computer , Application with computer system
Week 2	Computer classification [analog, digital, h• Input units, Output units ybrid], Main parts of a personal computer, Hardware: the structure of computer system ,

Week 3	Central processing units [CPU] , CPU components [ALU,RS,CU], CPU operations , Main memory, Primary storage, Type of main memory [RAM,ROM] Instruction format with memory , Secondary storage , Type of secondary storage
Week 4	Software Programs and application programs and utilities , System software and operating system and utilities ,Application packages.
Week 5	Software Programs and application programs and utilities ,System software and operating system and utilities, Application packages.
Week 6	➢ Number system • Decimal. Binary • Octal. • Hexadecimal
Week 7	➢ Addition and subtraction • binary • octal • Hexadecimal.
Week 8	➢ Logic gates. ➢ Boolean algebra and simplification and demorgan's
Week 9	➢ K-map. ➢ Combinational universal NAND and NOR logic.
Week 10	➢ Half-adder ➢ full-adder ➢ 4- bit parallel adder, and Subtract adder.
Week 11	➢ Decoder, encoder ➢ Multiplexer, and DE multiplexer.
Week 12	➢ Sequential logic circuits and Flip-flop, SR, D, and JK flip-flop.
Week 13	➢ Shift register 3-bit and 4-bit.
Week 14	➢ Binary counter 3-bit and 4-bit.
Week 15	**Preparatory Week**
Week 16	**Final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Logic gates.
Week 2	Lab 2: Boolean algebra and simplification and demorgan's
Week 3	Lab 3: K-map, Half-adder, full-adder
Week 4	Lab 4: 4-bit parallel adder, and Subtract adder

Week 5	Lab 5: Decoder, encoder, multiplexer, and de-multiplexer
Week 6	Lab 6: Sequential logic circuits and Flip-flop, SR, D, and JK flip-flop
Week 7	Shift registers 3-bit and 4-bit, Binary counter 3-bit and 4-bit.

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	**1.** Computer System Architecture M.Morris Mano	Yes
Recommended Texts	**2.** Digital fundamentals by Floyd, 2009	No
Websites	**3.** Fundamental of digital logic and Microcomputer design, fifth addition.	

APPENDIX:

GRADING SCHEME مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	مقبول بقرار	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required
Note:				

NB Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.